FIG. 1

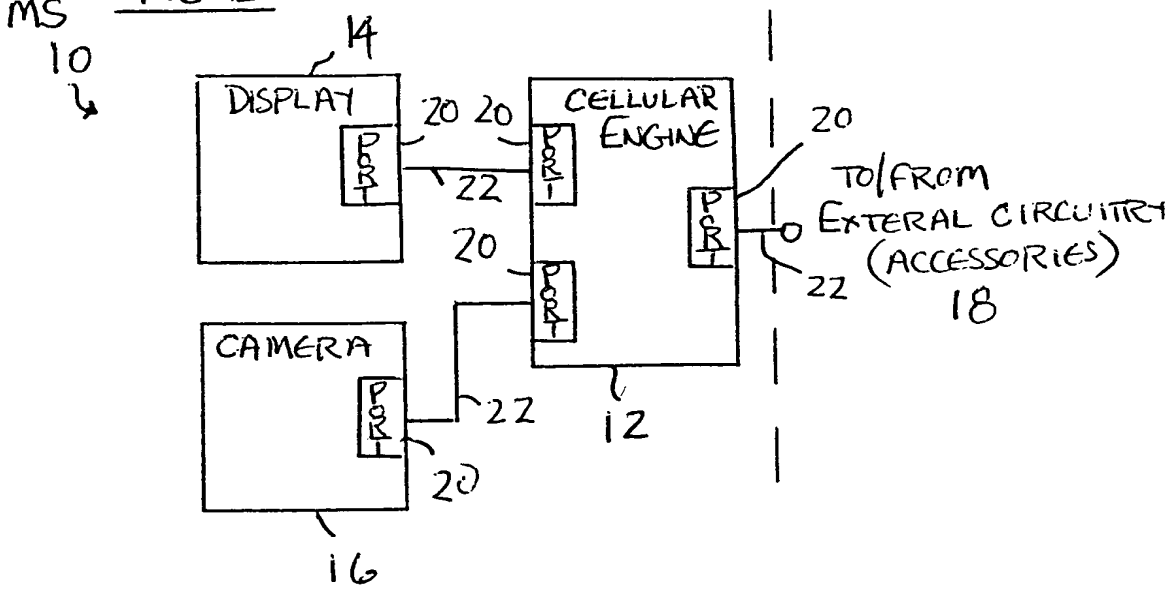

MS
10
14
DISPLAY
PORT
20
20
22
CELLULAR ENGINE
PORT 1
PORT
PORT
20
TO/FROM EXTERAL CIRCUITRY (ACCESSORIES)
18
22
20
CAMERA
PORT
22
12
20
16

FIG. 2

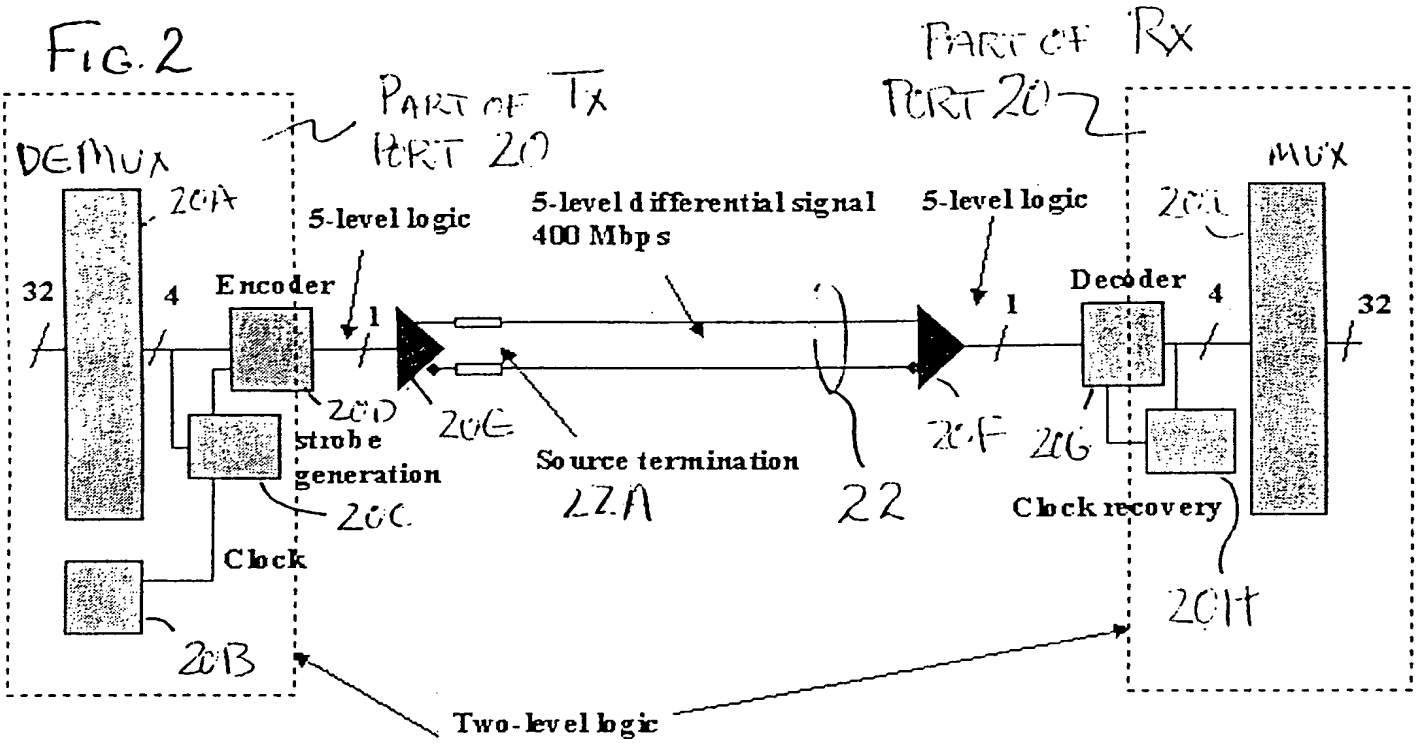

PART OF TX PORT 20
PART OF RX PORT 20
DEMUX
20A
32
4
Encoder
5-level logic
1
5-level differential signal 400 Mbps
5-level logic
1
Decoder
4
MUX
32
20D
strobe generation
20C
20E
Source termination
22A
22
20F
20G
Clock recovery
20H
Clock
20B
Two-level logic

FIG. 3A

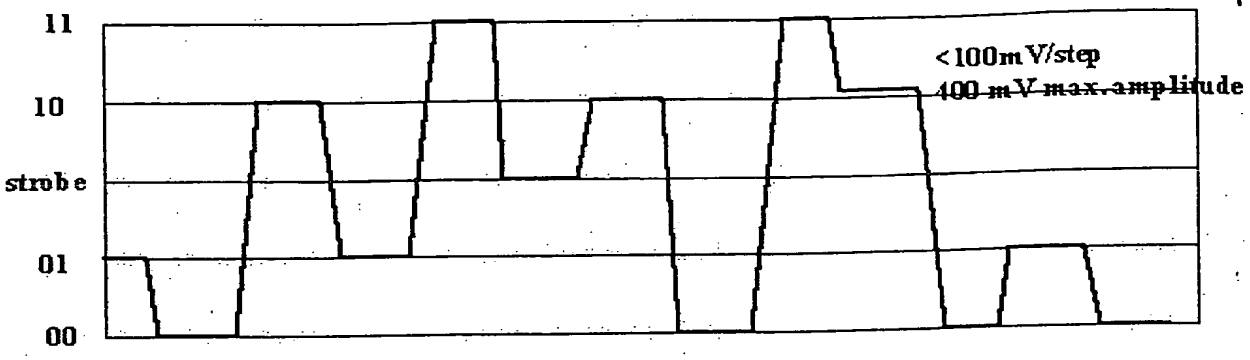


FIG. 3B

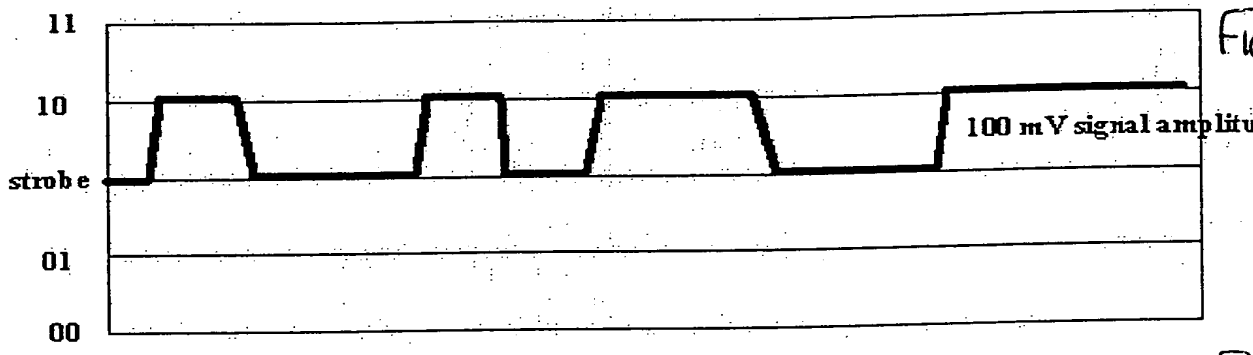
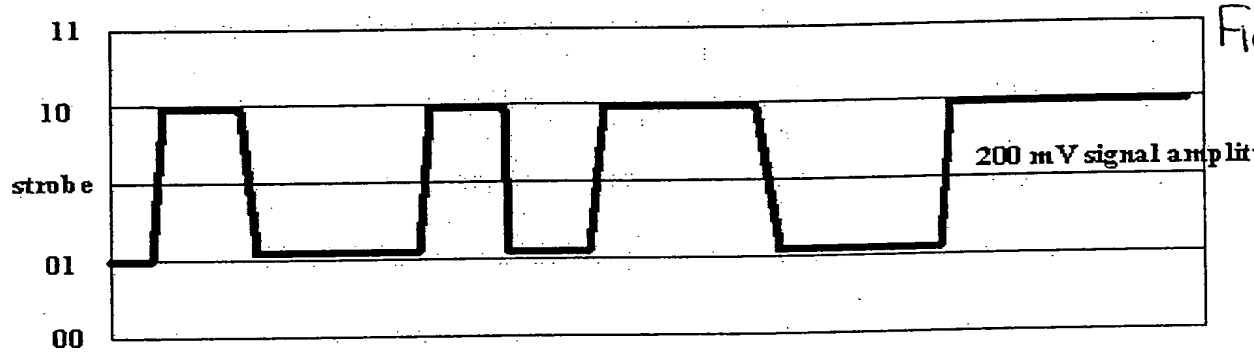


FIG. 3C



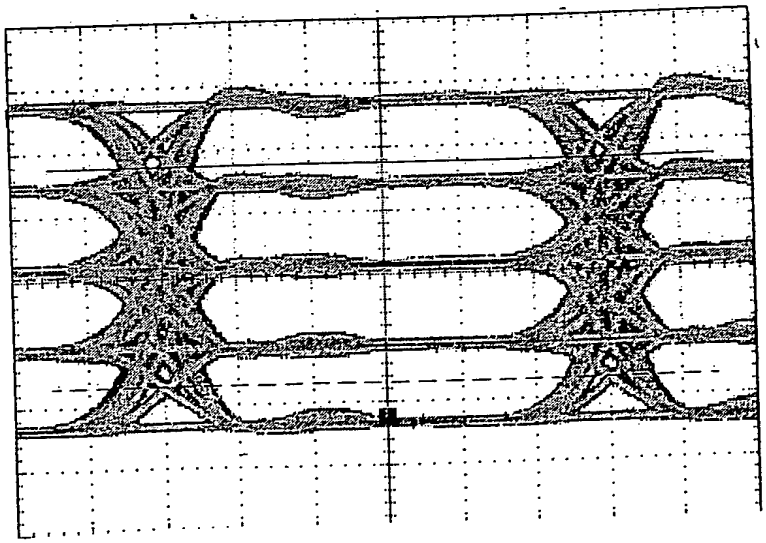


FIG. 4

667 MHz
1.5 GBaud
(PRIOR ART)

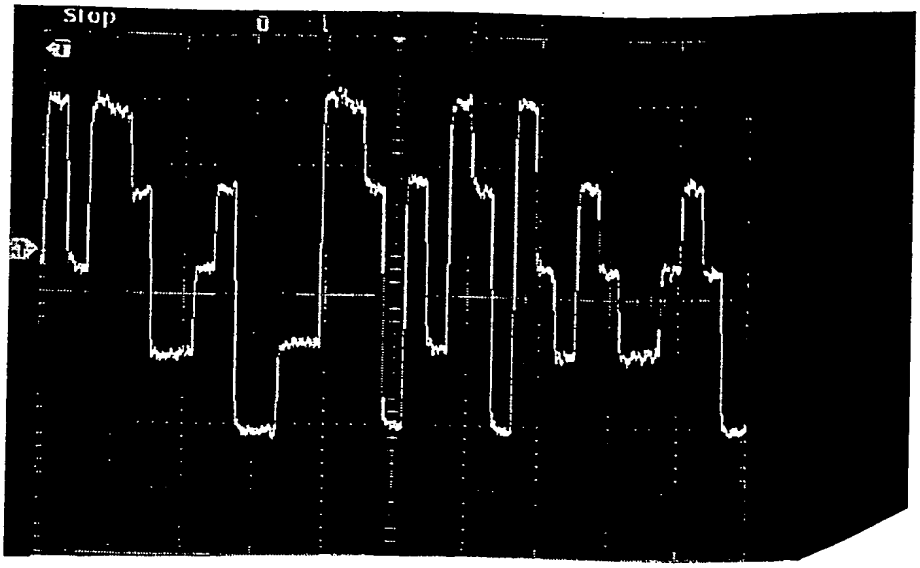


FIG. 5

30 MHz
60 MBaud
(PRIOR ART)

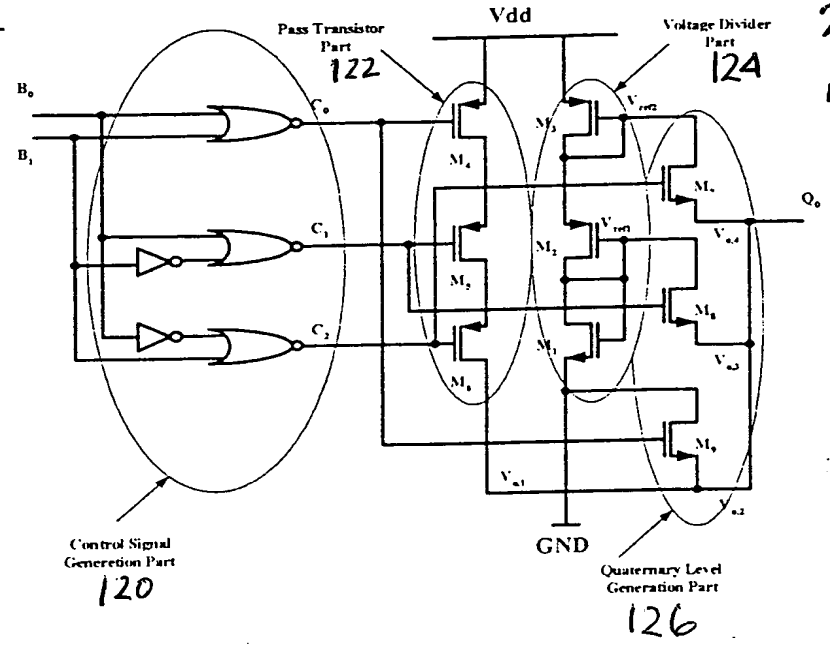
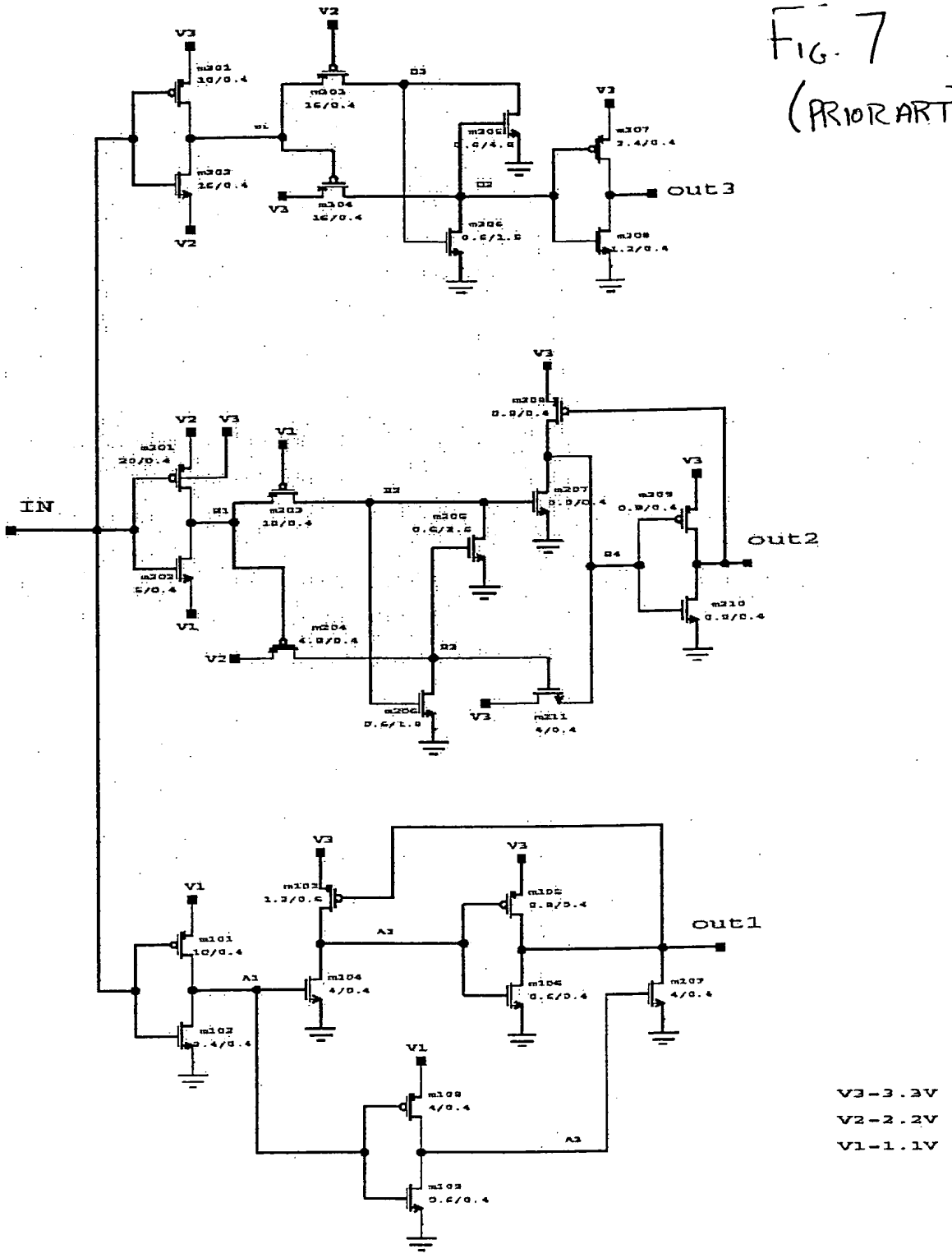


FIG. 6
(PRIOR ART)

B_i	B_{i+1}	C_0	C_1	C_2	Q_i
0	0	1	0	0	0
1	0	0	1	0	1
0	1	0	0	1	2
1	1	0	0	0	3

FIG. 7
(PRIOR ART)



V3 = 3.3V
V2 = 2.2V
V1 = 1.1V

FIG. 8

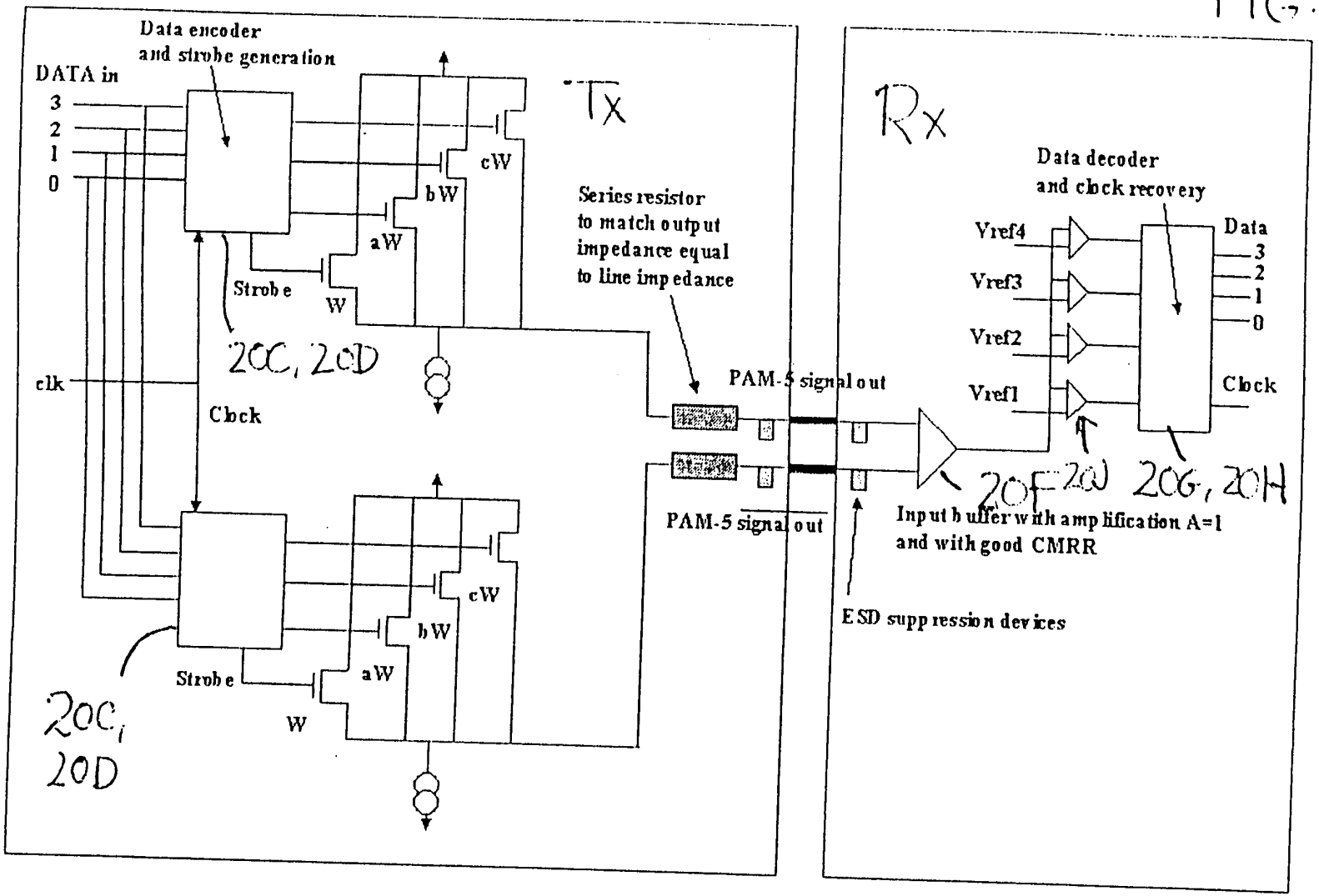
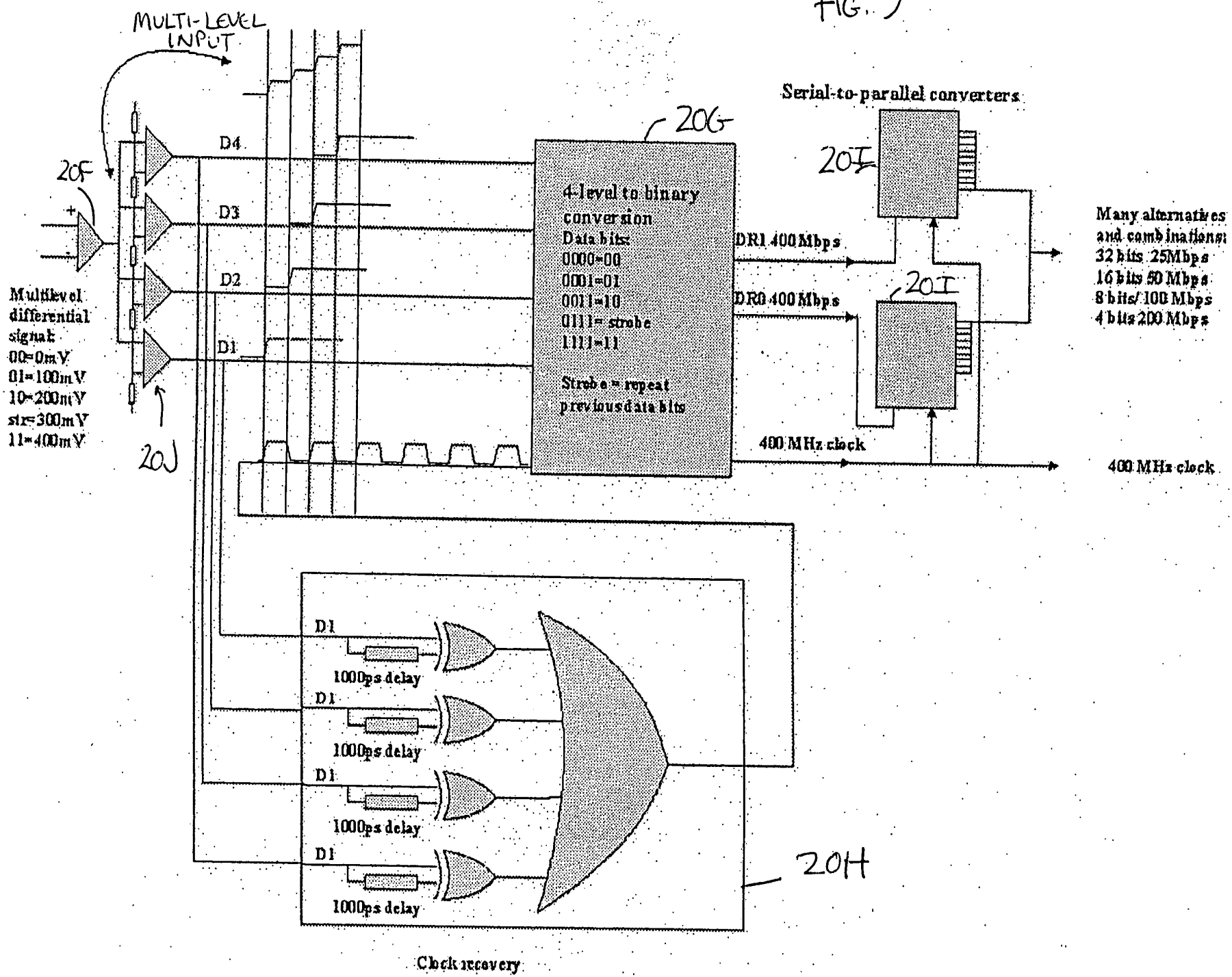

Data encoder
and strobe generation
DATA in
3
2
1
0
clk
Clock
Strobe
W
aW
bW
cW
20C, 20D
Tx
Series resistor
to match output
impedance equal
to line impedance
PAM-5 signal out
PAM-5 signal out
ESD suppression devices
Rx
Data decoder
and clock recovery
Vref4
Vref3
Vref2
Vref1
Data
3
2
1
0
Clock
20F-20J
20G, 20H
Input buffer with amplification A=1
and with good CMRR

FIG. 7


MULTI-LEVEL INPUT
20F
D4
D3
D2
D1
Multilevel differential signal:
00=0mV
01=100mV
10=200mV
11=300mV
11=400mV
20J
20G
4-level to binary conversion
Data bits:
0000=00
0001=01
0011=10
0111= strobe
1111=11
Strobe = repeat previous data bits
Serial-to-parallel converters
20E
20I
DR1 400Mbps
DR0 400Mbps
400 MHz clock
Many alternatives and combinations:
32 bits 25Mbps
16 bits 50 Mbps
8 bits/ 100 Mbps
4 bits 200 Mbps
400 MHz clock
D1
1000ps delay
D1
1000ps delay
D1
1000ps delay
D1
1000ps delay
20H
Clock recovery